CLAIMS

1. An oscillator circuit (100, 200, 300, 400, 500), comprising an oscillating element (110, 210, 310, 410, 510) and output means (115, 215, 315, 415) for outputting an oscillation frequency from said oscillating circuit, the circuit further comprising a signal delay means (120, 220, 320, 420, 520 ,525) which is arranged in series with the oscillating element and feeds the output signal back to the oscillating element, characterised in that the delay means (120, 220, 320, 420, 520 ,525) is tuneable with respect to the delay it provides.

2. The oscillator circuit (100, 200, 400) of claim 1, in which the oscillating element is an amplifier (110, 210, 410).

3. The oscillator circuit (100, 200, 400) of claim 2, further comprising a filter (130, 230, 430).

4. The oscillator circuit (100, 200) of claim 3, in which the delay means (120, 220) is a Delay Locked Loop.

5. The oscillator circuit (100) of claim 4, in which the filter (130) is a pass-band filter connected in series with the delay element (120), so as to filter the signal before it is fed back to the oscillating element (110), but after it has passed through the delay element.

6. The oscillator circuit (200) of claim 4, in which the filter (230) is a stop-band filter connected between the output means (215) and ground, so as to enable only the desired frequency to pass.

7. The oscillator circuit (400) of claim 3, in which the delay means (420) is a tuneable delay line comprising a control input, to which is connected the output signal from an amplitude detector (440), with the amplitude detector sampling the signal at a chosen point in the circuit (400) and controlling the

delay means so that a maximum output signal is obtained from the oscillator circuit

8. The oscillator circuit (400) of claim 7, in which the filter (430) is a stop-band filter connected between the output means (215) and ground, so as to enable only the desired frequency to pass.

9 The oscillator circuit (300, 500) of claim 1, in which the oscillating element is a voltage controlled oscillator (310, 510, 515).

10. The oscillator circuit (300) of claim 1 or 9, in which the delay means (320) is a Delay Locked Loop.

11. The oscillator circuit (500) of claim 1 or 9, in which the delay means (520, 525) is a tuneable delay line.

12. The oscillator circuit of claim 9 or 11, comprising at least a first and a second VCO (510, 515) and first and second tuneable delay lines (520,525), in which the VCO:s (510, 515), are connected in series via two branches, an "upper" and a "lower" branch, the output of the "lower" branch being used as input to the "upper" branch, and the output of the "upper" branch being used as input to the "lower" branch, with the delay means being connected one between each of the VCO:s, in series with them, so that the upper branch output of the first and second VCO are separated by the same phase distance as their respective lower branch outputs, suitably ninety degrees.